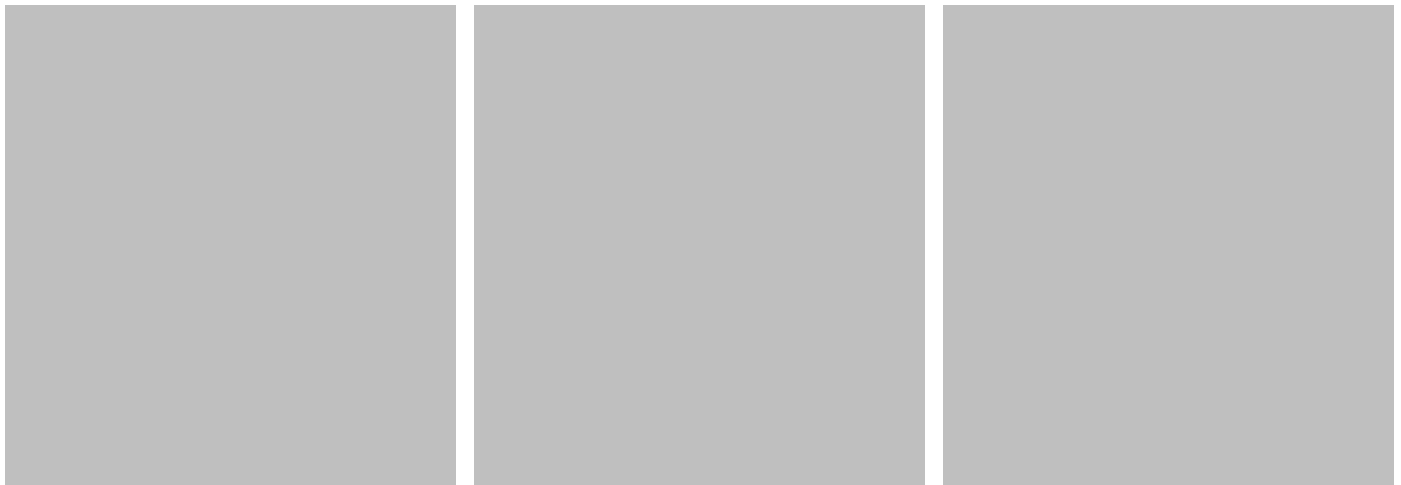




SLC 500™ Chassis-based Processors

(Catalog Numbers 1747-L511/L514, -L524, -L532, -L541, -L542, and -L543)

Product Data



The SLC 500 product line allows you to build just the right control system to meet your needs. We offer four chassis sizes, four power supplies, seven processors, and a variety of I/O modules. Additionally, we offer flexible communication options and programming and operator interface options.

The SLC 500 family of programmable controllers have expanded to meet a broader range of applications. From high-speed packaging and material handling applications to advanced processor control applications, Allen-Bradley offers the right processor for your job.

The SLC 5/03™ and SLC 5/04™ processors offer features previously found only on high-level PLCs. The SLC 500 processors provide a broad range of communication options, from DH-485, to RS-232, to DH+,™ Increased instruction support with ASCII, floating point math, and indirect addressing allows you to expand your application's capabilities.

Features and Benefits

Supports user memory sizes from 1K to 64K. By offering a wide range of user memory, SLC 500 modular processors can be used in a realm of applications.

Supports a variety of input and output modules. The 1746 modular I/O system offers over 50 types of modules, allowing you to customize your control solution to meet your application needs.

Supports I/O configurations of up to 3 chassis (30 local I/O slots). Provides you with the flexibility to expand I/O capacity as required.

Supports remote I/O and DeviceNet. The SLC 5/02 and above processors support up to 4096 discrete inputs and 4096 discrete outputs.

Provides superior system throughput. SLC 500 modular processors deliver fast overall system throughput times, providing fast response in high-speed applications.

Supports Data Highway Plus™ (DH+) communication. The SLC 5/04 processor provides communication and seamless integration into the larger Allen-Bradley PLC-5® network.

Supports DH-485 communication. Communication via the DH-485 network is available in every processor we ship, reducing your system cost for processor communication.

Provides a second channel for RS-232 communication for the SLC 5/03 and SLC 5/04 processors. This allows:

- dial up for remote monitoring and programming
- networking over modems for SCADA master/slave RTU applications
- an alternate connection for operator interfaces freeing up peer-to-peer network
- direct communication to ASCII devices such as bar code decoders and printers via a complete set of ASCII ladder instructions which simplify programming.

Provides user-selectable program security. The wide range of system protection capabilities allow you to secure user data and program files from changes.

Supports a host of third-party products through the Allen-Bradley Pyramid Solutions Program (PSP). PSP provides access to products and services that increase your application capabilities.

What's Inside..	Page
Features and Benefits	2
Overview of the Processors	3
System Throughput	6
Interrupt Subroutines	6
Communication Options	7
System Protection Options	9
I/O Usages	10
Programming Instructions	11
Indirect Addressing	18
Allen-Bradley Support	21
Specifications	22

Overview of the Processors

The SLC 500 processor product line offers four types of chassis-based processors.

SLC 5/01™ Processor (Catalog Number 1747-L511 or 1747-L514)

The SLC 5/01 processor offers the instruction set of the SLC 500 fixed controller in a modular hardware configuration. The SLC 5/01 processor provides:

- two choices of program memory size – 1K or 4K instructions
- control of up to 256 local I/O
- powerful ladder logic programming instruction set
- subroutines
- a DH-485 communication channel (peer-to-peer communication response to message commands only)
- capacitor backup for the -L511; battery backup for the -L514

SLC 5/02™ Processor (Catalog Number 1747-L524)

The SLC 5/02 processor expands beyond the SLC 5/01 processor capabilities by offering additional instructions, increased diagnostics, and peer-to-peer communication options. The SLC 5/02 processor provides:

- PID – used to provide closed loop process control
- indexed addressing
- control of up to 480 local I/O, expandable via Remote I/O and DeviceNet
- program memory size of 4K instructions
- interrupt capability
- user fault routines
- built-in DH-485 communication channel (initiation of peer-to-peer communication)
- ability to handle 32-bit signed math functions

SLC 5/03 Processor (Catalog Number 1747-L532)

The SLC 5/03 processor significantly increases performance by supplying system throughput times of 1 ms for a typical 1K user program. Now applications such as high-speed packaging, sorting, and material handling become more affordable. With the addition of online editing, the SLC 5/03 processor presents a positive solution for your continuous process application. A built-in RS-232 channel gives you the flexibility to connect to external intelligent devices without the need for additional modules.

The SLC 5/03 processor provides:

- program memory size of 16K
- control of up to 960 local I/O, expandable via Remote I/O and DeviceNet
- online programming (includes runtime editing)
- built-in RS-232 channel, supporting:
 - DF1 Full-Duplex for remote or point-to-point communication, or direct connection to IBM compatible programming devices
 - DF1 Half-Duplex Master/Slave for SCADA type communication
 - DH-485 (serves as a second DH-485 channel using a 1747-PIC or direct connection to IBM compatible programming devices)
 - ASCII for connection to other ASCII devices, such as bar code readers, printers, and weigh scales
- built-in DH-485 channel
- built-in real-time clock/calendar
- 1 ms Selectable Timed Interrupt (STI)
- 0.50 ms Discrete Input Interrupt (DII)
- advanced math features – trigonometric, PID, exponential, floating point, and the compute instruction
- indirect addressing
- flash PROM provides firmware upgrades without physically changing EPROMS
- keyswitch – RUN, REMote, PROGram (clear faults)

SLC 5/04 Processor (Catalog Number 1747-L541, -L542, or -L543)

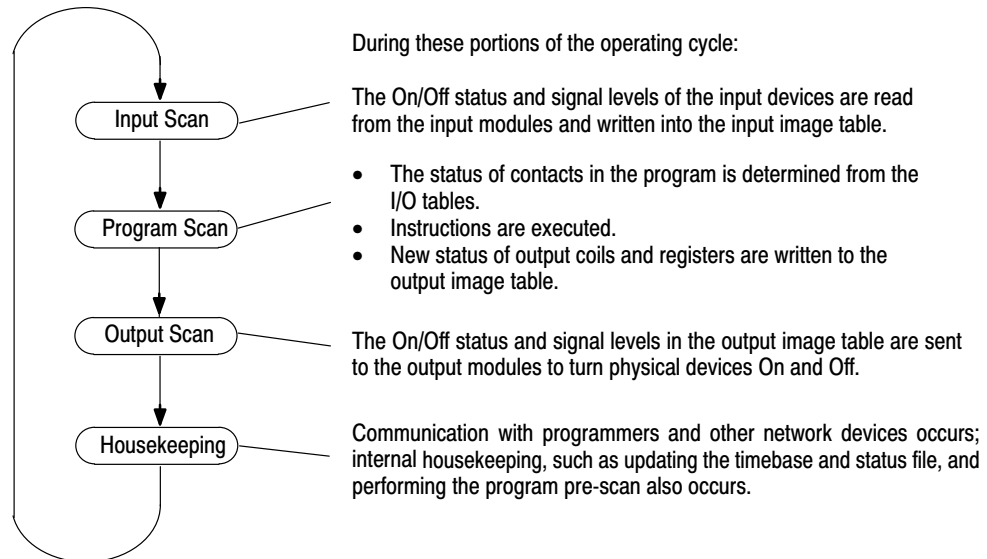
The SLC 5/04 processor provides the baseline functionality of the SLC 5/03 processor plus DH+ communication. Communication via DH+ takes place three times faster than DH-485 communication, providing you with increased performance levels. In addition, the SLC 5/04 processor runs approximately 15% faster than the SLC 5/03 processor, yielding system thru-put times of 0.90 ms for a typical 1K user program. The variety of memory sizes allow you to closely match your application need; 16K, 32k, or 64K.

The SLC 5/04 processor provides:

- program memory sizes of 16K, 32K, or 64K
- high-speed performance – 0.90 ms/K typical
- control of up to 960 local I/O, expandable via Remote I/O and DeviceNet
- online programming (includes runtime editing)
- built-in DH+ channel, supporting:
 - high-speed SLC 5/04 to SLC 5/04 communication
 - messaging capability between PLCs[®] and SLCs[™]
 - monitoring capabilities to PLC-2[®], PLC-3[®], PLC-5, and PLC-5/250[™] processors
- built-in RS-232 channel, supporting:
 - DF1 Full-Duplex for remote or point-to-point communication, or direct connection to IBM compatible programming devices
 - DF1 Half-Duplex Master/Slave for SCADA type communication
 - DH-485 (serves as a second DH-485 channel using a 1747-PIC or direct connection to IBM compatible programming devices)
 - ASCII for connection to other ASCII devices, such as bar code readers, printers, and weigh scales
- passthru capability to PanelView[™] 550 and PanelView 900
- remote I/O passthru
- built-in real-time clock/calendar
- 1 ms Selectable Timed Interrupt (STI)
- 0.50 ms Discrete Input Interrupt (DII)
- advanced math features – trigonometric, PID, exponential, floating point, and the compute instruction
- indirect addressing
- flash PROM provides firmware upgrades without physically changing EPROMS
- keyswitch – RUN, REMote, PROGram (clear faults)

System Throughput

When your application requires high-speed processing it requires more than just fast instruction or program scan times. It requires speed from the time an input is read until the time an output is turned on. The SLC 500 processors improve performance in every phase of system throughput, from input and output scans, to program scans and housekeeping functions.



Interrupt Subroutines

The following interrupt subroutines allow you to provide predetermined responses to special events in an application.

Selectable Timed Interrupt

This function allows you to interrupt the scan of the processor automatically, on a periodic basis, in order to scan a specified subroutine file. When using an SLC 5/02 processor, the Selectable Timed Interrupt (STI) timebase can be adjusted in 10 ms increments. When using an SLC 5/03 or SLC 5/04 processor, the STI timebase can be adjusted in 1 ms increments.

Discrete Input Interrupt

Use the Discrete Input Interrupt (DII) for high-speed processing applications or any application that needs to respond to an event quickly. This function allows the processor to execute a ladder subroutine when the input bit pattern of a discrete I/O card matches a compare value that you programmed. The discrete input interrupt is examined every 100 μ s asynchronous to the ladder program scan. You may also specify the number of counts (matches) to occur before subroutine execution.

I/O Event Interrupt

This function allows the 1746-BAS (BASIC) module to interrupt the normal processor operating cycle in order to scan a specified subroutine file. Use this interrupt with SLC 5/02, SLC 5/03, and SLC 5/04 processors.

Communication Options

The SLC 500 processors support different types of communication options. The following sections describe the available physical connections and protocol options used by the SLC 500 processors.

Physical Connection Options

Data Highway Plus (DH+) channel offers:

- communication rates up to 57.6K baud
- maximum network length of 3,048 m (10,000 ft)
- Belden 9463 (blue hose) cable connection between nodes (daisy chain connection)
- built-in isolation

DH-485 channel offers:

- configurable communication rates up to 19.2K baud
- electrical isolation via the 1746-AIC
- maximum network length of 1219 m (4,000 ft)
- RS-485 electrical specifications
- Belden 9842 cable connection between nodes (daisy chain connection)

RS-232 channel offers:

- communication rates up to 19.2K baud
- maximum distance between devices is 15.24 m (50 ft)
- RS-232C electrical specifications
- modem support
- built-in isolation

The table below summarizes the SLC 500 processor channel connections.

Processor	Physical Communication Channel		
	DH-485	RS-232	DH+
SLC 5/01	DH-485 protocol	NA	NA
SLC 5/02	DH-485 protocol	NA	NA
SLC 5/03 Channel 0	NA	DH-485, ^① DF1 Full-Duplex, DF1 Half-Duplex Master/Slave, and ASCII protocols	NA
Channel 1	DH-485 protocol	NA	NA
SLC 5/04 Channel 0	NA	DH-485, ^① DF1 Full-Duplex, DF1 Half-Duplex Master/Slave, and ASCII protocols	NA
Channel 1	NA	NA	DH+ protocol

NA (Not Applicable)

^① A 1747-PIC is required when connecting to a DH-485 channel.

Protocol Options

Data Highway Plus (DH+) Protocol

The Data Highway Plus protocol is used by the PLC-5 family of processors and the SLC 5/04 processor. This protocol is similar to DH-485, except that it can support up to 64 devices (nodes) and can run at faster communication (baud) rates.

DH-485 Protocol

The SLC 500 processors have a DH-485 channel that supports the DH-485 communication network. This network is a multi-master, token-passing network protocol capable of supporting up to 32 devices (nodes). This protocol allows:

- monitoring of data and processor status, along with program uploading and downloading of any device on the network from one location
- SLC processors to pass data to each other (peer-to-peer communication)
- operator interface devices on the network to access data from any SLC processor on the network

DF1 Full-Duplex Protocol

DF1 Full-Duplex protocol (also referred to as DF1 point-to-point protocol) allows two devices to communicate with each other at one a time. This protocol allows:

- transmission of information across modems (dial-up, leased line, and radio)
- communication to occur between Allen-Bradley products and third-party products

DF1 Half-Duplex Protocol (Master and Slave)

DF1 Half-Duplex protocol provides a multi-drop single master/multiple slave network capable of supporting up to 255 devices (nodes). This protocol also provides modem support and is ideal for SCADA (Supervisory Control and Data Acquisition) applications because of the network capability.

ASCII Protocol

The ASCII protocol provides connection to other ASCII devices, such as bar code readers, weigh scales, printers, and other intelligent devices.

System Protection Options

The SLC 500 family of processors offer a number of hardware and software security features that allow you to protect your system from unauthorized changes to program or data files. The different types of protection are:

Types of Protection	SLC 5/01	SLC 5/02	SLC 5/03 and SLC 5/04
Password	•	•	•
Future Access (OEM Lock)	•	•	•
Program Owner	•	•	•
Program Files	NA	NA	•
Data Table Files	•	•	•
Memory Module Data File Overwrite	NA	NA	•
Memory Module Program Compare	NA	NA	•
Memory Module Write Protection	NA	NA	•
Force Protection	NA	NA	•
Keyswitch	NA	NA	•
Communication Channel Protection	NA	NA	•

NA (Not Applicable)

I/O Usages

The SLC 500 family of processors support a variety of I/O modules, allowing you to exactly match your application. The following table lists the various types of I/O modules and their compatibility with the SLC 500 processors.

I/O Module	SLC 5/01	SLC 5/02	SLC 5/03 and SLC 5/04
1746-Discrete Input/Output AC/DC	•	•	•
1746-Analog Modules	•	•	•
1746-NT4, 1746-NR4 Thermocouple and RTD Input Modules	•	•	•
1747-SN Remote I/O Scanner Module	NA	•	•
1746-SDN DeviceNet Scanner Module	NA	•	•
1747-DSN Distributed I/O Scanner Module	•	•	•
1746-BAS Basic Module	•	•	•
1747-KE DH-485/RS232 KE Module	•	•	•
1746-HSCE High-Speed Counter Encoder Module	NA	•	•
1746-HSTP1 Stepper Controller Module	NA	•	•
1746-HS IMC 110 Servo Controller Module	•	•	•

NA (Not Applicable)

Programming Instructions

The following programming instructions are used with the SLC 500 processors. Included are instruction execution times (μ s) for the processors when the instruction is True and instruction execution times (μ s) when floating point math is used.

Basic Instructions

Instruction Mnemonic and Name	Execution Times (μ s)				Function – Conditional Instructions Input or Output
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
XIC Examine if Closed	4	2.4	0.44	0.37	Conditional instruction. True when bit is on (1).
XIO Examine if Open	4	2.4	0.44	0.37	Conditional instruction. True when bit is off (0).
OTE Output Energize	18	11	0.63	0.56	Output instruction. True (1) when conditions preceding it are true. False when conditions preceding it go false.
OTL Output Latch	19	11	0.63	0.56	Output instruction. Addressed bit goes true (1) when conditions preceding the OTL instruction are true. When conditions go false, OTL remains true until the rung containing an OTU instruction with the same address goes true.
OTU Output Unlatch	19	11	0.63	0.56	Output instruction. Addressed bit goes false (0) when conditions preceding the OTU instruction are true. Remains false until the rung containing an OTL instruction with the same address goes true.
OSR One-Shot Rising	34	20	10.80	9.10	Conditional instruction. Makes rung true for one scan upon each false-to-true transition of conditions preceding it in the rung.
TON Timer On-Delay	135	83	1.40	1.31	Counts time intervals when conditions preceding it in the rung are true. Produces an output when accumulated value (count) reaches the preset value.
TOF Timer Off-Delay	140	86	1.40	1.31	Counts time intervals when conditions preceding it in the rung are false. Produces an output when accumulated value (count) reaches the preset value.
RTO Retentive Timer	140	86	1.40	1.31	This is an On-Delay timer that retains its accumulated value when: – Rung conditions go false. – The mode changes to program from run or test. – The processor loses power. – A fault occurs.
CTU Count Up	111	69	1.40	1.31	Counts up for each false-to-true transition of conditions preceding it in the rung. Produces an output when accumulated value (count) reaches the preset value.
CTD Count Down	111	69	1.40	1.31	Counts down for each false-to-true transition of conditions preceding it in the rung. Produces an output when accumulated value (count) reaches the preset value.
RES Reset	40	26	1.40	1.31	Used with timers and counters. When conditions preceding it in the rung are true, the RES instruction resets the accumulated value and control bits of the timer or counter.

Comparison Instructions

Instruction Mnemonic and Name	Execution Times (μs)/ Floating Point (μs) ^①				Function – Conditional (Input) Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
EQU Equal	60	38	1.25/12.94	1.12/12.5	Instruction is true when source A = source B.
NEQ Not Equal	60	38	1.25/13.25	1.12/12.18	Instruction is true when source A ≠ source B.
LES Less Than	60	38	1.25/13.19	1.12/13.94	Instruction is true when source A < source B.
LEQ Less Than or Equal	60	38	1.25/13.19	1.12/13.93	Instruction is true when source A ≤ source B.
GRT Greater Than	60	38	1.25/14.82	1.12/12.62	Instruction is true when source A > source B.
GEQ Greater Than or Equal	60	38	1.25/14.81	1.12/14.31	Instruction is true when source A ≥ source B.
MEQ Masked Comparison for Equal	75	47	38/NA	22.75/NA	Compares 16-bit data of a source address to 16-bit data at a reference address through a mask. If the values match, the instruction is true.
LIM Limit Test	NA	45	1.95/22.81	1.68/20.19	True/false status of the instruction depends on how a test value compares to specified low and high limits.

NA (Not Applicable)

^① Floating point times do not apply to SLC 5/03 OS300 processors.

Math Instructions

Instruction Mnemonic and Name	Execution Times (μs)/ Floating Point (μs) ^①				Function – Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
ADD Add	122	76	1.70/38.44	1.50/18.22	When rung conditions are true, the ADD instruction adds source A to source B and stores the result in the destination.
SUB Subtract	125	77	1.70/38.19	1.50/19.50	When rung conditions are true, the SUB instruction subtracts source B from source A and stores the result in the destination.
MUL Multiply	230	140	20/39.05	17.75/ 21.94	When rung conditions are true, the MUL instruction multiplies source A by source B and stores the result in the destination.
DIV Divide	400	242	23/57.56	25.9/23.27	When rung conditions are true, the DIV instruction divides source A by source B and stores the result in the destination and the math register.
DDV Double Divide	650	392	33/NA	29.6/NA	When rung conditions are true, the DDV instruction divides the contents of the math register by the source and stores the result in the destination and the math register.
NEG Negate	110	68	1.70/12.38	1.5/11.87	When rung conditions are true, the NEG instruction changes the sign of the source and places it in the destination.
CLR Clear	40	26	1.70/6.62	1.5/5.94	When rung conditions are true, the CLR instruction clears the destination to zero.
SQR Square Root	NA	162	32/70.00	28.8/18.87	When rung conditions are true, the SQR instruction calculates the square root of the source and places the result in the destination.

NA (Not Applicable)

^① Floating point times do not apply to SLC 5/03 OS300 processors.

Math Instructions continued

Instruction Mnemonic and Name ^②	Execution Times (μs)/ Floating Point (μs) ^①				Function – Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
SCL Scale	NA	480	32/NA	33.06/NA	When rung conditions are true, the SCL instruction multiplies the source by a specified rate. The result is added to an offset value and placed in the destination.
SCP Scale with Parameters	NA	NA	33.10/ 196.10	29.85/ 94.15	Produces a scaled output value that has a linear relationship between the input and scaled values.
CPT Compute	NA	NA	8.8/NA ^③	7.7/NA ^③	Evaluates an expression and stores the result in the destination.
SWP Swap	NA	NA	24 + 13.09 per word	22.6 + 12.13 per word	Swaps the low and high bytes of a specified number of words in a bit integer, ASCII, or string file.
ABS Absolute Value	NA	NA	9.95/ 5.20	8.60/ 4.35	Calculates the absolute value of the source and places the result in the destination.
XPY X to the Power of Y Register/Data	NA	NA	699.30/NA	335.10/NA	Raises a value to a power and stores the result in the destination.
LOG Log to the Base 10	NA	NA	390.80/NA	54.55/NA	Takes the log base 10 of the value in the source and stores the result in the destination.
LN Natural Log	NA	NA	392.00/NA	51.35/NA	Takes the natural log of the value in the source and stores it in the destination.
SIN Sine	NA	NA	311.95/NA	38.05/NA	Takes the sine of a number and stores the result in the destination.
COS Cosine	NA	NA	310.90/NA	37.20/NA	Takes the cosine of a number and stores the result in the destination.
TAN Tangent	NA	NA	406.35/NA	43.00/NA	Takes the tangent of a number and stores the result in the destination.
ASN Arc Sine	NA	NA	483.05/NA	41.45/NA	Takes the arc sine of a number and stores the result (in radians) in the destination.
ACS Arc Cosine	NA	NA	510.85/NA	51.90/NA	Takes the arc cosine of a number and stores the result (in radians) in the destination.
ATN Arc Tangent	NA	NA	387.05/NA	40.15/NA	Takes the arc tangent of a number and stores the result (in radians) in the destination.

NA (Not Applicable)

① Floating point times do not apply to SLC 5/03 OS300 processors.

② Applies to SLC 5/03 OS302 and SLC 5/04 OS401 processors.

③ To get the total execution time for a CPT instruction, take the CPT execution time plus each additional math instruction execution time, plus the number of math instructions times 3.01.
For example if a CPT instruction calls one ADD and one SUB instruction the calculation is:
 $8.8 + 1.70 + 1.70 + 2(3.01) = 18.22$

Data Handling Instructions

Instruction Mnemonic and Name	Execution Times (μs)/ Floating Point (μs) ^①				Function – Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
TOD Convert to BCD	200	122	38/NA	34.06/NA	When rung conditions are true, the TOD instruction converts the source value to BCD and stores it in the math register or the destination.
FRD Convert from BCD	223	136	31/NA	23.88/NA	When rung conditions are true, the FRD instruction converts a BCD value in the math register or the source to an integer and stores it in the destination.
RAD Degrees to Radians ^②	NA	NA	31.80/NA	24.65/NA	When rung conditions are true, RAD converts degrees (source) to radians and stores the result in the destination.
DEG Radians to Degrees ^②	NA	NA	32.80/NA	24.70/NA	When rung conditions are true, DEG converts radians (source) to degrees and stores the result in the destination.
DCD Decode	80	50	10/NA	8.88/NA	When rung conditions are true, the DCD instruction decodes 4-bit value (0 to 16), turning on the corresponding bit in 16-bit destination.
COP File Copy	45 + 21 per word	29 + 13 per word	30 + 2.20 per word/ NA	20.2 + 2.0 per word/ NA	When rung conditions are true, the COP instruction copies a user-defined source file to the destination file.
FLL File Fill	37 + 14 per word	25 + 8 per word	28 + 2 per word/ NA	21.9 + 2.5 per word/ NA	When rung conditions are true, the FLL instruction loads a source value into a specified number of elements in a user-defined file.
MOV Move	20	14	1.25/12.19	1.12/11.44	When rung conditions are true, the MOV instruction moves a copy of the source to the destination.
MVM Masked Move	115	71	19/NA	17.40/NA	When rung conditions are true, the MVM instruction moves a copy of the source through a mask to the destination.
AND And	87	55	1.70/NA	1.5/NA	When rung conditions are true, sources A and B of the AND instruction are ANDed bit by bit and stored in the destination.
OR Inclusive Or	87	55	1.70/NA	1.5/NA	When rung conditions are true, sources A and B of the OR instruction are ORed bit by bit and stored in the destination.
XOR Exclusive Or	87	55	1.70/NA	1.5/NA	When rung conditions are true, sources A and B of the XOR instruction are Exclusive ORed bit by bit and stored in the destination.
NOT Not	66	42	1.70/NA	1.5/NA	When rung conditions are true, the source of the NOT instruction is NOTed bit by bit and stored in the destination.
FFL First In First Out (FIFO) Load (FFL)	NA	150	58/NA	40.75/NA	The FFL instruction loads a word into a FIFO stack on successive false-to-true transitions. The FFU unloads a word from the stack on successive false-to-true transitions. The first word loaded is the first to be unloaded.
FFU Unload (FFU)	NA	150 + 11 per word	79 + 2.20 per word/ NA	60 + 2 per word/ NA	
LFL Last In First Out (LIFO) Load (LFL)	NA	150	58/NA	40.70/NA	The LFL instruction loads a word into a LIFO stack on successive false-to-true transitions. The LFU unloads a word from the stack on successive false-to-true transitions. The last word loaded is the first to be unloaded.
LFU Unload (LFU)	NA	180	66/NA	34.70/NA	

NA (Not Applicable)

^① Floating point times do not apply to SLC 5/03 OS300 processors.

^② Applies to SLC 5/03 OS302 and SLC 5/04 OS401 processors.

Program Flow Instructions

Instruction Mnemonic and Name	Execution Times (μs)				Function – Conditional or Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
JMP Jump to Label	38	23	44.45	37.44	Output instruction. When rung conditions are true, the JMP instruction causes the program scan to jump forward or backward to the corresponding LBL instruction.
LBL Label	2	4	0.25	0.18	This is the target of the correspondingly numbered JMP instruction.
JSR Jump to Subroutine	46	28	131.0	112.0	Output instruction. When rung conditions are true, the JSR instruction causes the processor to jump to the targeted subroutine file.
SBR Subroutine	2	4	0.25	0.18	Placed as first instruction in a subroutine file. Identifies the subroutine file.
RET Return from Subroutine	34	20	23	20.0	Output instruction, placed in subroutine. When rung conditions are true, the RET instruction causes the processor to resume program execution in the main program file or the previous subroutine file.
MCR Master Control Reset	10	6	4	3.0	Output instruction. Used in pairs to inhibit or enable a zone within a ladder program.
TND Temporary End	32	22	12	13.05	Output instruction. When rung conditions are true, the TND instruction stops the program scan, updates I/O, and resumes scanning at rung 0 of the main program file.
SUS Suspend	12	7	12	10.31	Output instruction, used for troubleshooting. When rung conditions are true, the SUS instruction places the controller in the Suspend Idle mode. The suspend ID number is placed in word S:7 and the program file number is placed in S:8.
IIM Immediate Input with Mask	372	340	51.85	51.0	When conditions preceding it in the rung are true, the IIM instruction is enabled and interrupts the program scan to write a word of masked external input data to the input data file.
IOM Immediate Output with Mask	475	465	70.90	75.74	When conditions preceding it in the rung are true, the IOM instruction is enabled and interrupts the program scan to read a word of data from the output data file and transfer the data through a mask to the corresponding external outputs.

Application Specific Instructions

Instruction Mnemonic and Name	Execution Times (μs)				Function – Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
BSL Bit Shift Left BSR Bit Shift Right	144 +24 per word	89 + 14 per word	50 + 2.30 per word	31.5 + 2.31 per word	On each false-to-true transition, these instructions load a bit of data into a bit array, shift the pattern of data through the array, and unload the end bit of data. The BSL shifts data to the left and the BSR shifts data to the right.
SQO Sequencer Output	225	137	70	44.1	On successive false-to-true transitions, the SQO moves a step through the programmed sequencer file, transferring step data through a mask to a destination word.
SQC Sequencer Compare	225	137	60	33.2	On successive false-to-true transitions, the SQC moves a step through the programmed sequencer file, comparing the data through a mask to a source word or file for equality.
SQL Sequencer Load	NA	135	56	33.2	On successive false-to-true transitions, the SQL moves a step through the sequencer file, loading a word of source data into the current element of the sequencer file.

NA (Not Applicable)

Communication Instructions

Instruction Mnemonic and Name	Execution Times (μs)				Function – Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
MSG Message Read/Write	NA	180	203	183	This instruction transfers data from one node to another on the communication network. When the instruction is enabled, message transfer is pending. Actual data transfer takes place at the end of the scan.
SVC Service Communications	NA	240	240	200	When conditions preceding it in the rung are true, the SVC instruction interrupts the program scan to execute the service communication portion of the operating cycle.

NA (Not Applicable)

Proportional Integral Derivative Instruction

Instruction Mnemonic and Name	Execution Times (μs)				Function – Output Instruction
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
PID Proportional Integral Derivative	NA	3600	272	169.82	This instruction is used to control physical properties such as temperature, pressure, liquid level, or flow rate of process loops.

NA (Not Applicable)

ASCII Instructions^①

Instruction Mnemonic and Name	Execution Times (μs)		Function – Output Instructions
	SLC 5/03	SLC 5/04	
ABL Test Buffer for Line	129.9	156.0	Determines the number of characters in the buffer, up to and including the end-of-line characters (termination).
ACB Number of Characters in Buffer	140.7	131.0	Determines the total characters in the buffer.
ACI String to Integer	86.62	56.0	Converts an ASCII string to an integer value.
ACL ASCII Clear Receive and/or Send Buffer	367.5	332.8	Clears the ASCII buffer.
ACN String Concatenate	69.4 + 2.1 per character	56 + 2.5 per character	Combines two strings using ASCII strings as operands.
AEX String Extract	56.2 + 4.7 per character	43.4 + 4.0 per character	Creates a new string by taking a portion of an existing string and linking it to a new string.
AHL ASCII Handshake Lines	138.7	115.1	Sets or resets the RS-232 Data Terminal Ready and Request to Sender handshake control lines for the modem.
AIC Integer to String	103.4	110.0	Converts an integer value to an ASCII string.
ARD ASCII Read Characters	181.8	151.0	Reads characters from the buffer and stores them in a string.
ARL ASCII Read Line	190.0	156.0	Reads characters from the buffer up to and including the end-of-line characters and stores them in a string.
ASC String Search	53.4 + 1.8 per character	43.5 + 2.5 per character	Searches an existing string for an occurrence of the source string.
ASR ASCII String Compare	49.69	43.5	Compares two ASCII strings.
AWA ASCII Write with Append	365.5	307.8	Adds the two appended characters set from the ASCII configuration menu.
AWT ASCII Write	263.8	217.3	Writes characters from a source string to a display device.

^① Only SLC 5/03 OS301, OS302 and SLC 5/04 OS400, OS401 processors use these instructions.

Interrupt Routine Instructions

Instruction Mnemonic and Name		Execution Times (μs)				Function – Output Instructions
		SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	
STD	Selectable Timed Disable	NA	9	4	3.56	Associated with the Selectable Timed Interrupt function. STD and STE are used to prevent an STI from occurring during a portion of the program; STS initiates an STI.
STE	Selectable Timed Enable	NA	9	5	5.0	
STS	Selectable Timed Start	NA	72	58	44.38	
IIE	I/O Interrupt Enable	NA	42	16	10.44	The IIE, IID, and RPI instructions are used with specialty I/O modules capable of generating an I/O interrupt.
IID	I/O Interrupt Disable	NA	39	6	5.81	
RPI	Reset Pending I/O Interrupt	NA	240	78 + 60 per added slot	91 + 56 per added slot	
REF	I/O Refresh	NA	240	240	200	When conditions preceding it in the rung are true, the REF instruction interrupts the program scan to execute the I/O scan (write outputs-service comms-read inputs). The program scan then resumes.
INT	Interrupt Subroutine	NA	0	0.25	0.18	Associated with STI interrupts and I/O event-driven interrupts.

NA (Not Applicable)

Indirect Addressing

The following sections describe how indirect addressing affects the execution time of instructions in the SLC 5/03 OS302 and SLC 5/04 OS401 processors. The timing for an indirect address is affected by:

- the form of the indirect address
- whether the indirect address is a source or destination parameter
- whether indirect addressing is used in either a COP, FLL, FFL/FFU, LFL/LFU, BSR, BSL, or MVM instruction
- whether indirect addressing is used in either an XIC, XIO, OTU, OTL, OTE, or OSR instruction

For the address forms in the table on the next page, you can substitute the following file types:

For an Integer (N)

- Input (I)
- Output (O)
- Bit (B)
- Floating Point (F)
- ASCII (A)

For a String (ST)

- Control (R)
- Counter (C)
- Timer (T)

Execution Times for Word-Level Indirect Addresses

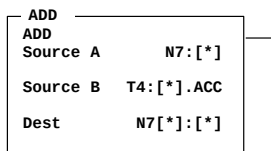
For most types of instructions that contain an indirect address(es), look up the form of the indirect address in the table below and add that time to the execution time of the instruction.

Address Form ^①	Source Operand (μs)		Destination Operand (μs)		If used in a file type instruction	
	SLC 5/03	SLC 5/04	SLC 5/03	SLC 5/04	SLC 5/03	SLC 5/04
N7:[*]	65.1	56.15	63.10	54.20	76.35	66.75
ST12:[*].[*]	69.45	60.00	67.45	58.05	80.70	70.60
ST12:[*].0	74.65	59.60	72.65	57.65	85.90	70.20
ST12:0.[*]	74.65	59.60	72.65	57.65	85.90	70.20
N[*]:[*]	105.90	89.40	131.50	112.55	138.75	118.70
N[*]:0	111.10	89.00	136.70	112.15	143.95	118.30
ST[*]:[*].[*]	110.25	93.25	135.85	116.40	143.10	122.55
ST[*]:[*].0	115.45	92.85	141.05	116.00	148.30	122.15
ST[*]:0.[*]	115.45	92.85	141.05	116.00	148.30	122.15
ST[*]:0.0	120.65	92.45	146.25	115.60	153.50	121.75
#N7:[*]	73.05	59.35	64.65	57.30	86.80	69.80
#ST12:[*].[*]	77.40	63.20	69.00	61.15	91.15	73.65
#ST12:[*].0	82.60	62.80	74.20	60.75	96.35	73.25
#ST12:0.[*]	82.60	62.80	74.20	60.75	96.35	73.25
#N[*]:[*]	110.95	92.95	133.40	114.40	146.65	121.35
#N[*]:0	116.15	92.55	138.60	114.00	151.85	120.95
#ST[*]:[*].[*]	115.30	96.80	137.75	118.25	151.00	125.20
#ST[*]:[*].0	120.50	96.40	142.95	117.85	156.20	124.80
#ST[*]:0.[*]	120.50	96.40	142.95	117.85	156.20	124.80
#ST[*]:0.0	125.70	96.00	148.15	117.45	161.40	124.40

^① [*] indicates that an indirect reference is substituted.

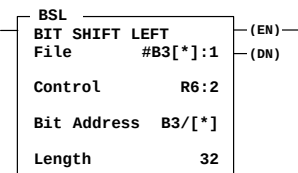
Examples

SLC 5/03



ADD 1.70
Source A 65.10
Source B 74.65
Destination 131.50
 272.95 μs

SLC 5/04



BSL 31.5 + (2)2.31 = 36.12
File 120.95
Bit Address 77.80
 234.87 μs

Execution Times for Bit-Level Indirect Addresses

Indirect bit addresses are based on the form of the indirect address and the type of bit instruction. Use the following two tables to calculate the execution time of a bit instruction.

Address Form	Additional Time (μs)	
	SLC 5/03	SLC 5/04
B3/[*]	96.70	77.80
B3:1/[*]	96.70	77.80
B3:[*]/[*]	91.50	72.80
ST12:[*].[*]/[*]	100.65	76.65
ST12:[*].[*]/0	100.85	76.25
ST12:[*].0/[*]	100.85	76.25
ST12:[*].0/0	105.85	75.85
ST12:0.[*]/0	105.85	75.85
ST12:0.0/[*]	105.85	75.85
B[*]/[*]	171.50	141.40
B[*]:1/[*]	171.50	141.40
B[*]:[*]/[*]	166.30	141.80
ST[*]:[*].[*]/[*]	170.65	145.65
ST[*]:[*].[*]/0	175.85	145.25
ST[*]:[*].0/[*]	175.85	145.25
ST[*]:[*].0/0	181.05	144.85
ST[*]:0.[*]/[*]	175.85	145.25
ST[*]:0.[*]/0	181.05	144.85
ST[*]:0.0/[*]	181.05	144.85
ST[*]:0.0/0	186.25	144.45

Instruction Execution Times

Instruction	Execution Time (μs)	
	SLC 5/03	SLC 5/04
XIC	10.20	8.72
XIO	14.65	12.76
OTU	6.30	5.45
OTL	9.35	5.40
OTE	6.25	5.50
OSR	10.50	8.10

Example

To calculate the execution time of an XIC at B3/[N7:0] using an SLC 5/03 processor add the following:

$$10.20 + 96.70 = 106.90$$

Allen-Bradley Support

In today's competitive environment, when you buy any product, you expect that product to meet your needs. You also expect the manufacturer of that product to back it up with the kind of customer service and product support that will prove you made a wise purchase.

As the people who design, engineer and manufacture your Industrial Automation Control equipment, Allen-Bradley has a vested interest in your complete satisfaction with our products and services.

Allen-Bradley offers support services worldwide, with 75 Sales/Support offices, 512 authorized Distributors and 260 authorized Systems Integrators located throughout the United States, plus Allen-Bradley representatives in every major country in the world.

Contact your local Allen-Bradley representative for:

- sales and order support
- product technical training
- warranty support
- support service agreements

Specifications

The following table summarizes the detailed specifications for the SLC 500 processor family:

Specification	SLC 5/01 (1747-L511, -L514)	SLC 5/02 (1747-L524)	SLC 5/03 (1747-L532)	SLC 5/04		
				1747-L541	1747-L542	1747-L543
Program Memory	1K or 4K Instructions	4K Instructions	12K Words	12K Words	28K Words	60K Words
Additional Data Storage	0	0	up to 4K Words	up to 4K Words	up to 4K Words	up to 4K Words
Max. Local I/O Capacity	256 Discrete	480 Discrete	960 Discrete	960 Discrete	960 Discrete	960 Discrete
Remote I/O	NA	Maximum number dependent on system power supply loading and program memory size. (4096 inputs and 4096 outputs)				
Max. Local Chassis/Slots	3/30	3/30	3/30	3/30	3/30	3/30
Programming	PLC-500 A.I., APS, and HHT	PLC-500 A.I., APS, and HHT	PLC-500 A.I. and APS	PLC-500 A.I. and APS	PLC-500 A.I. and APS	PLC-500 A.I. and APS
Programming Instructions	52	71	99	99	99	99
Typical Scan Time ^①	8 ms/K	4.8 ms/K	1 ms/K	0.9 ms/K	0.9 ms/K	0.9 ms/K
Bit Execution (XIC)	4 μs	2.4 μs	0.44 μs	0.37 μs	0.37 μs	0.37 μs

^① The scan times are typical for a 1K ladder logic program consisting of simple ladder logic and communication servicing. Actual scan times depend on your program size, instructions used, and the communication protocol.

The following table summarizes the communication options for the SLC 500 processor family.

Communication	Receive	Receive or Initiate
DH-485	SLC 5/01	SLC 5/02, SLC 5/03, SLC 5/04
RS-232 (DF1 Full-Duplex, DF1 Half-Duplex Master/Slave, DH-485, or ASCII)	SLC 5/01 ^①	SLC 5/02, ^① SLC 5/03, SLC 5/04
Data Highway Plus	SLC 5/01 ^{②③}	SLC 5/02, ^{②③} SLC 5/03, ^② SLC 5/04

^① A 1747-PIC is required when connecting to the DH-485 channel.

^② A 1785-KA5 is required.

^③ Receive is only through the 1785-KA5.

The following table summarizes the general specifications for the SLC 500 processor family:

Description	Specification
Power Supply Loading at 5V dc	350 mA for SLC 5/01, and SLC 5/02 processor
	500 mA for the SLC 5/03 processor
	1.0A for the SLC 5/04 processor
Power Supply Loading at 24V dc	105 mA for SLC 5/01, and SLC 5/02 processor
	175 mA for the SLC 5/03 processor
	200 mA for the SLC 5/04 processor
Program Scan Hold-up Time after Loss of Power	20 ms to 3 s (dependent on power supply loading)
Clock/Calendar Accuracy (applicable only to SLC 5/03 and SLC 5/04 processors)	+ or – 54 sec/month @ 25° C (77° F) + or – 81 sec/month @ 60° C (140° F)
Noise Immunity	NEMA Standard ICS 2-230
Vibration	Displacement: 0.015 inch, peak-to-peak at 5–57 Hz
	Acceleration: 2.5Gs at 57–2000 Hz
Shock (operating)	30Gs
Ambient Temperature Rating	Operating: 0 to + 60° C (32° F to 140° F) Storage: –40° C to 85° C (–40° F to 185° F)
Humidity	5 to 95% without condensation
Certification	UL listed/ CSA approved Class 1, Groups A, B, C or D, Division 2 CE marked for all applicable directives

The following table summarizes the available memory back up options for the SLC 500 processors. EEPROM and UVPROM memory modules provide non-volatile memory back-up. Flash EPROMs (Flash Erasable Programmable Read Only Memory) combine the versatility of EEPROMs with the security of UVPROMs.

Memory Back Up Option	SLC 5/01 (1747-511/514)	SLC 5/02 1747-L524	SLC 5/03 1747-L532	SLC 5/04		
				1747-L541	1747-L542	1747-L543
EEPROM	1747-M1, 1747-M2	1747-M2	NA	NA	NA	NA
UVPROM	1747-M3, 1747-M4	1747-M4	NA	NA	NA	NA
Flash	NA	NA	1747-M11 1747-M12 (OS302 only)	1747-M11 1747-M12 (OS401 only)	1747-M11 1747-M12 (OS401 only)	1747-M11 1747-M12 (OS401 only)

NA (Not Applicable)

SLC, SLC 500, SLC 5/01, SLC 5/02, SLC 5/03, SLC 5/04, DH+, Data Highway Plus, PanelView, and PLC-5/250 are trademarks of Allen-Bradley Company, Inc.
PLC, PLC-2, PLC-3, and PLC-5 are registered trademarks of Allen-Bradley Company, Inc.



ALLEN-BRADLEY
A ROCKWELL INTERNATIONAL COMPANY

Allen-Bradley has been helping its customers improve productivity and quality for 90 years. A-B designs, manufactures and supports a broad range of control and automation products worldwide. They include logic processors, power and motion control devices, man-machine interfaces and sensors. Allen-Bradley is a subsidiary of Rockwell International, one of the world's leading technology companies.



With major offices worldwide.

Algeria • Argentina • Australia • Austria • Bahrain • Belgium • Brazil • Bulgaria • Canada • Chile • China, PRC • Colombia • Costa Rica • Croatia • Cyprus • Czech Republic • Denmark • Ecuador • Egypt • El Salvador • Finland • France • Germany • Greece • Guatemala • Honduras • Hong Kong • Hungary • Iceland • India • Indonesia • Israel • Italy • Jamaica • Japan • Jordan • Korea • Kuwait • Lebanon • Malaysia • Mexico • New Zealand • Norway • Oman • Pakistan • Peru • Philippines • Poland • Portugal • Puerto Rico • Qatar • Romania • Russia-CIS • Saudi Arabia • Singapore • Slovakia • Slovenia • South Africa, Republic • Spain • Switzerland • Taiwan • Thailand • The Netherlands • Turkey • United Arab Emirates • United Kingdom • United States • Uruguay • Venezuela • Yugoslavia

World Headquarters, Allen-Bradley, 1201 South Second Street, Milwaukee, WI 53204 USA, Tel: (1) 414 382-2000 Fax: (1) 414 382-4444